**What is Claimed is:**

1. A microelectronic package comprising:

a first microelectronic substrate including a first face and a first AC-coupled interconnect element on the first face;

a second microelectronic substrate including a second face and a second AC-coupled interconnect element on the second face; and

a buried solder bump that extends between the first and second faces and that is at least partially buried beneath at least one of the first and second faces to maintain the first and second AC-coupled interconnect elements in closely spaced apart relation.

2. A microelectronic package according to Claim 1 wherein the first AC-coupled interconnect element comprises a first capacitor plate and wherein the second AC-coupled interconnect element comprises a second capacitor plate.

3. A microelectronic package according to Claim 1 wherein the first AC-coupled interconnect element comprises a first inductor and wherein the second AC-coupled interconnect element comprises a second inductor.

4. A microelectronic package according to Claim 1 wherein the first AC-coupled interconnect element comprises a first combined inductive and capacitive element and wherein the second AC-coupled interconnect element comprises a second combined inductive and capacitive element.

5. A microelectronic package according to Claim 1 further comprising a trench in the second face, including a trench floor beneath the second face, the buried solder bump extending between the trench floor and the first face.

6. A microelectronic package according to Claim 1 further comprising:

a first trench in the first face, including a first trench floor beneath the first face; and

a second trench in the second face, including a second trench floor beneath the second face;

wherein the buried solder bump extends between the first trench floor and the second trench floor.

7. A microelectronic package according to Claim 5 further comprising:

a first solder bump pad on the trench floor and a second solder bump pad on the first face, the buried solder bump extending between the first solder bump pad and the second solder bump pad.

8. A microelectronic package according to Claim 6 further comprising:

a first solder bump pad on the first trench floor and a second solder bump pad on the second trench floor, the buried solder bump extending between the first solder bump pad and the second solder bump pad.

9. A microelectronic package according to Claim 1 wherein the first microelectronic substrate is an integrated circuit and wherein the second microelectronic substrate is a second level package for the integrated circuit.

10. A microelectronic package according to Claim 9 wherein the first AC-coupled interconnect element comprises a first inductor and wherein the second AC-coupled interconnect element comprises a second inductor having greater inductance than the first inductor.

11. A microelectronic package according to Claim 1 further comprising a DC offset compensating receiver in at least one of the first and second substrates that is coupled to the corresponding at least one of the first and second AC-coupled interconnect elements.

12. A microelectronic package according to Claim 3 further comprising a current mode driver in at least one of the first and second substrates that is coupled to the corresponding at least one of the first and second inductors.

13. A microelectronic package according to Claim 4 further comprising a current mode driver in at least one of the first and second substrates that is coupled to

the corresponding at least one of the first and second combined inductive and capacitive elements.

14. A microelectronic package according to Claim 1 wherein the buried solder bump is further configured to transfer DC power between the first and second substrates.

15. A microelectronic package according to Claim 1 wherein the first and second AC-coupled interconnect elements comprise first and second AC-coupled signal interconnect elements.

16. A microelectronic package according to Claim 1 wherein the first and second AC-coupled interconnect elements comprise first and second AC-coupled power interconnect elements.

17. A microelectronic package according to Claim 3 further comprising a first mutual inductance coupling element on the first inductor opposite the first substrate, and a second mutual inductance coupling element on the second inductor opposite the second substrate.

18. A microelectronic package according to Claim 4 further comprising a first mutual inductance coupling element on the first combined inductive and capacitive element opposite the first substrate, and a second mutual inductance coupling element on the second combined inductive and capacitive element opposite the second substrate.

19. A microelectronic package comprising:

a microelectronic substrate including a face and an AC-coupled interconnect element on the face; and

a buried solder bump that is at least partially buried beneath the first face.

20. A microelectronic package according to Claim 19 wherein the AC-coupled interconnect element comprises a capacitor plate.

21. A microelectronic package according to Claim 19 wherein the AC-coupled interconnect element comprises an inductor.

22. A microelectronic package according to Claim 19 wherein the AC-coupled interconnect element comprises a combined inductive and capacitive element.

23. A microelectronic package according to Claim 19 further comprising a trench in the face, and including a trench floor beneath the face, the buried solder bump being on the trench floor.

24. A microelectronic package according to Claim 23 further comprising:

a solder bump pad on the trench floor, the buried solder bump being on the first solder bump pad.

25. A microelectronic package according to Claim 19 wherein the AC-coupled interconnect element comprises an AC-coupled signal interconnect element.

26. A microelectronic package according to Claim 19 further comprising:

a DC power supply circuit that is electrically coupled to the buried solder bump.

27. A microelectronic package according to Claim 19 further comprising a DC offset compensating receiver in the substrate that is coupled to the AC-coupled interconnect element.

28. A microelectronic package according to Claim 21 further comprising a current mode driver in the substrate that is coupled to the inductor.

29. A microelectronic package according to Claim 22 further comprising a current mode driver in the substrate that is coupled to the combined inductive and capacitive element.

30. A microelectronic package according to Claim 21 further comprising a mutual inductance coupling element on the inductor opposite the substrate.

31. A microelectronic package according to Claim 22 further comprising a mutual inductance coupling element on the combined inductive and capacitive element opposite the substrate.

32. A microelectronic package comprising:

a microelectronic substrate including a face and a trench in the face, including a trench floor beneath the face;

an AC-coupled interconnect element on the face; and

a solder bump pad on the trench floor.

33. A microelectronic package according to Claim 32 further comprising:

a solder bump on the solder bump pad.

34. A microelectronic package according to Claim 32 wherein the AC-coupled interconnect element comprises a capacitor plate.

35. A microelectronic package according to Claim 32 wherein the AC-coupled interconnect element comprises an inductor.

36. A microelectronic package according to Claim 32 wherein the AC-coupled interconnect element comprises a combined inductive and capacitive element.

37. A microelectronic package according to Claim 32 wherein the AC-coupled interconnect element comprises an AC-coupled signal interconnect element.

38. A microelectronic package according to Claim 32 further comprising:

a DC power supply circuit that is electrically coupled to the buried solder bump.

39. A microelectronic package according to Claim 32 further comprising a DC offset compensating receiver in the substrate that is coupled to the AC-coupled interconnect element.

40. A microelectronic package according to Claim 35 further comprising a current mode driver in the substrate that is coupled to the inductor.

41. A microelectronic package according to Claim 36 further comprising a current mode driver in the substrate that is coupled to the combined inductive and capacitive element.

42. A microelectronic package according to Claim 35 further comprising a mutual inductance coupling element on the inductor opposite the substrate.

43. A microelectronic package according to Claim 36 further comprising a mutual inductance coupling element on the combined inductive and capacitive element opposite the substrate.

44. A microelectronic package comprising:

a first microelectronic substrate including a first face;

a first inductor on the first face;

a digital signal driver in the first microelectronic substrate that is configured to drive the first inductor with a digital signal;

a second microelectronic substrate including a second face;

a second inductor on the second face that is closely spaced apart from the first inductor; and

a digital signal receiver in the second microelectronic substrate that is configured to receive the digital signal from the digital signal driver via inductive coupling between the first and second inductors.

45. A microelectronic package according to Claim 44 further comprising:

a buried solder bump that extends between the first and second faces and that is at least partially buried beneath at least one of the first and second faces to maintain the first and second inductors in closely spaced apart relation.

46. A microelectronic package according to Claim 44 wherein the first and second inductors also include capacitance associated therewith.

47. A microelectronic package according to Claim 44 wherein the first microelectronic substrate is an integrated circuit and wherein the second microelectronic substrate is a second level package for the integrated circuit.

48. A microelectronic package according to Claim 47 wherein the second inductor has greater inductance than the first inductor.

49. A microelectronic package according to Claim 44 wherein the digital signal receiver is a DC offset compensating digital signal receiver.

50. A microelectronic package according to Claim 44wherein the digital signal driver is a current mode digital signal driver.

51. A microelectronic package according to Claim 44 further comprising a first mutual inductance coupling element on the first inductor opposite the first substrate, and a second mutual inductance coupling element on the second inductor opposite the second substrate.

52. A microelectronic package comprising:

a first microelectronic substrate including a first face and a first AC-coupled interconnect element on the first face;

a second microelectronic substrate including a second face and a second AC-coupled interconnect element on the second face;

a solder bump having a solder bump thickness and that extends between the first and second substrates; and

means for maintaining the first and second AC-coupled interconnect elements spaced apart from one another by a distance that is less than the solder bump thickness.

53. A microelectronic package according to Claim 52 wherein the first AC-coupled interconnect element comprises a first capacitor plate and wherein the second AC-coupled interconnect element comprises a second capacitor plate.

54. A microelectronic package according to Claim 52 wherein the first AC-coupled interconnect element comprises a first inductor and wherein the second AC-coupled interconnect element comprises a second inductor.

55. A microelectronic package according to Claim 52 wherein the first AC-coupled interconnect element comprises a first combined inductive and capacitive element and wherein the second AC-coupled interconnect element comprises a second combined inductive and capacitive element.

56. A microelectronic package according to Claim 52 wherein the first microelectronic substrate is an integrated circuit and wherein the second microelectronic substrate is a second level package for the integrated circuit.

57. A microelectronic package according to Claim 54 wherein the first AC-coupled interconnect element comprises a first inductor and wherein the second AC-coupled interconnect element comprises a second inductor having greater inductance than the first inductor.

58. A microelectronic package according to Claim 52 further comprising a DC offset compensating receiver in at least one of the first and second substrates and coupled to the corresponding at least one of the first and second AC-coupled interconnect elements.

59. A microelectronic package according to Claim 54 further comprising a current mode driver in at least one of the first and second substrates and coupled to the corresponding at least one of the first and second inductors.

60. A microelectronic package according to Claim 55 further comprising a current mode driver in at least one of the first and second substrates that is coupled to the corresponding at least one of the first and second combined inductive and capacitive elements.

61. A microelectronic package according to Claim 52 wherein the first and second AC-coupled interconnect elements comprise first and second AC-coupled signal interconnect elements.

62. A microelectronic package according to Claim 52 wherein the first and second AC-coupled interconnect elements comprise first and second AC-coupled power interconnect elements.

63. A microelectronic package according to Claim 54 further comprising a first mutual inductance coupling element on the first inductor opposite the first substrate, and a second mutual inductance coupling element on the second inductor opposite the second substrate.

64. A microelectronic package according to Claim 55 further comprising a first mutual inductance coupling element on the first combined inductive and capacitive element opposite the first substrate, and a second mutual inductance coupling element on the second combined inductive and capacitive element opposite the second substrate.

65. A microelectronic package comprising:

a first microelectronic substrate including a first face and a first AC-coupled interconnect element on the first face;

a second microelectronic substrate including a second face and a second AC-coupled interconnect element on the second face; and

an electrically conductive structure that extends between the first and second substrates and that is configured to maintain the first and second AC-coupled interconnect elements spaced apart from one another and is also configured to transfer DC power between the first and second substrates.

66. A microelectronic package according to Claim 65 wherein the electrically conductive structure comprises a solder bump.

67. A microelectronic package according to Claim 65 wherein the first AC-coupled interconnect element comprises a first capacitor plate and wherein the second AC-coupled interconnect element comprises a second capacitor plate.

68. A microelectronic package according to Claim 65 wherein the first AC-coupled interconnect element comprises a first inductor and wherein the second AC-coupled interconnect element comprises a second inductor.

69. A microelectronic package according to Claim 65 wherein the first AC-coupled interconnect element comprises a first combined inductive and capacitive element and wherein the second AC-coupled interconnect element comprises a second combined inductive and capacitive element.

70. A microelectronic package according to Claim 65 wherein the first microelectronic substrate is an integrated circuit and wherein the second microelectronic substrate is a second level package for the integrated circuit.

71. A microelectronic package according to Claim 68 wherein the first AC-coupled interconnect element comprises a first inductor and wherein the second AC-coupled interconnect element comprises a second inductor having greater inductance than the first inductor.

72. A microelectronic package according to Claim 65 wherein the first and second AC-coupled interconnect elements comprise first and second AC-coupled signal interconnect elements.

73. A microelectronic package according to Claim 68 further comprising a first mutual inductance coupling element on the first inductor opposite the first substrate, and a second mutual inductance coupling element on the second inductor opposite the second substrate.

74. A microelectronic package according to Claim 69 further comprising a first mutual inductance coupling element on the first combined inductive and capacitive element opposite the first substrate, and a second mutual inductance

coupling element on the second combined inductive and capacitive element opposite the second substrate.

75. An electrical connector comprising:

a first mating connector substrate including a first mating connector face;

a first array of inductors on the first mating face;

a second mating connector substrate including a second mating connector face; and

a second array of inductors on the second mating face;

the first and second mating connector substrates being configured to maintain the first and second mating connector faces in closely spaced apart relation to provide inductive coupling between corresponding inductors in the first and second arrays of inductors.

76. An electrical connector according to Claim 75 further comprising at least one pin and at least one corresponding pin clip on at least one of the first and second mating connector substrates and configured to maintain the first and second mating connector faces in closely spaced apart relation.

77. An electrical connector according to Claim 75 wherein the inductors in the first and second arrays of inductors also include capacitance associated therewith.